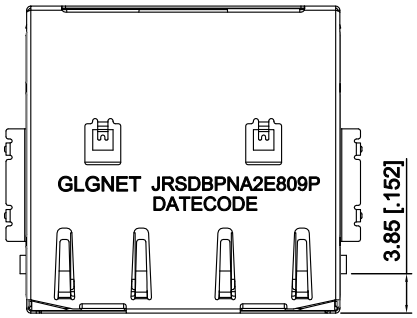
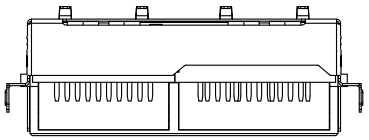
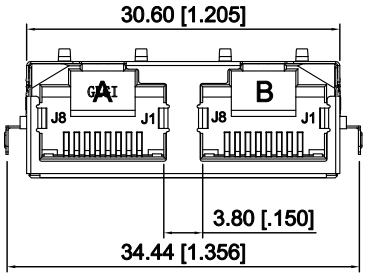
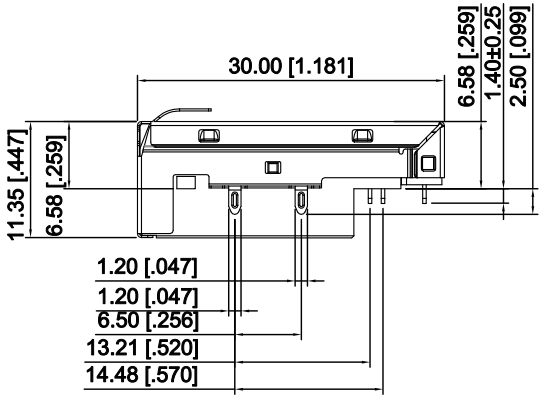
Mechanical

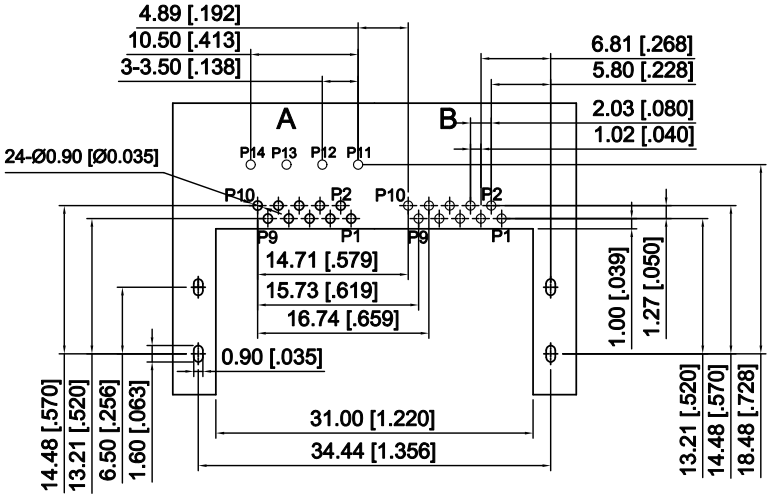
NO.	ECN NO.	DESCRIPTION	REV.	DRAW	DATE





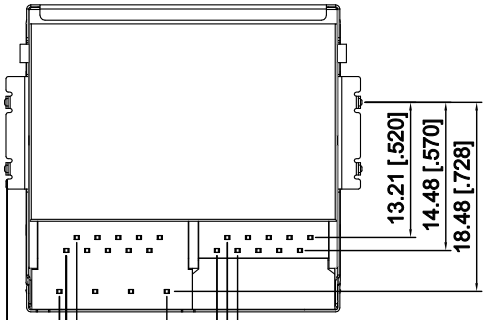


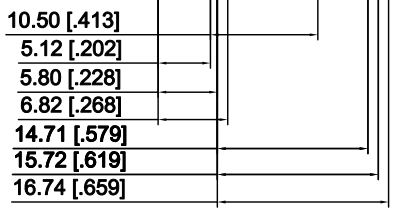




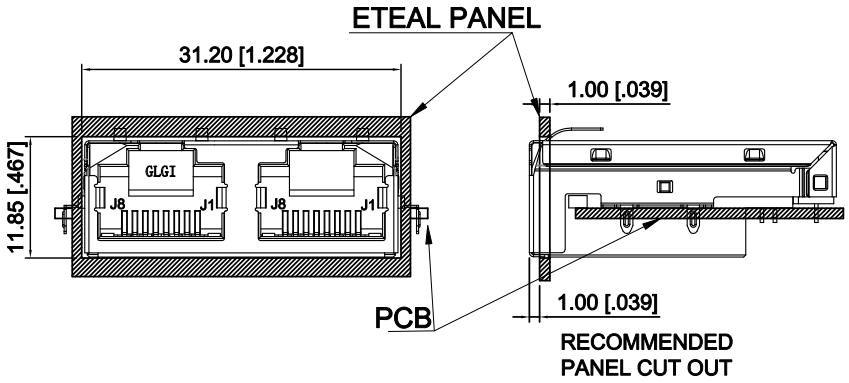
RECOMMENDED P.C.B LAYOUT
TOP VIEW (COMPONENT SIDE)

Dimensions Tolerance:
All PCB LAYOUT
Tolerances:±0.05[.002]





GoldPlating	Option
1.8μ"	☐
3μ"	☐
6μ"	■
15μ"	☐
30μ"	☐
50μ"	☐



RECOMMENDED
PANEL CUT OUT

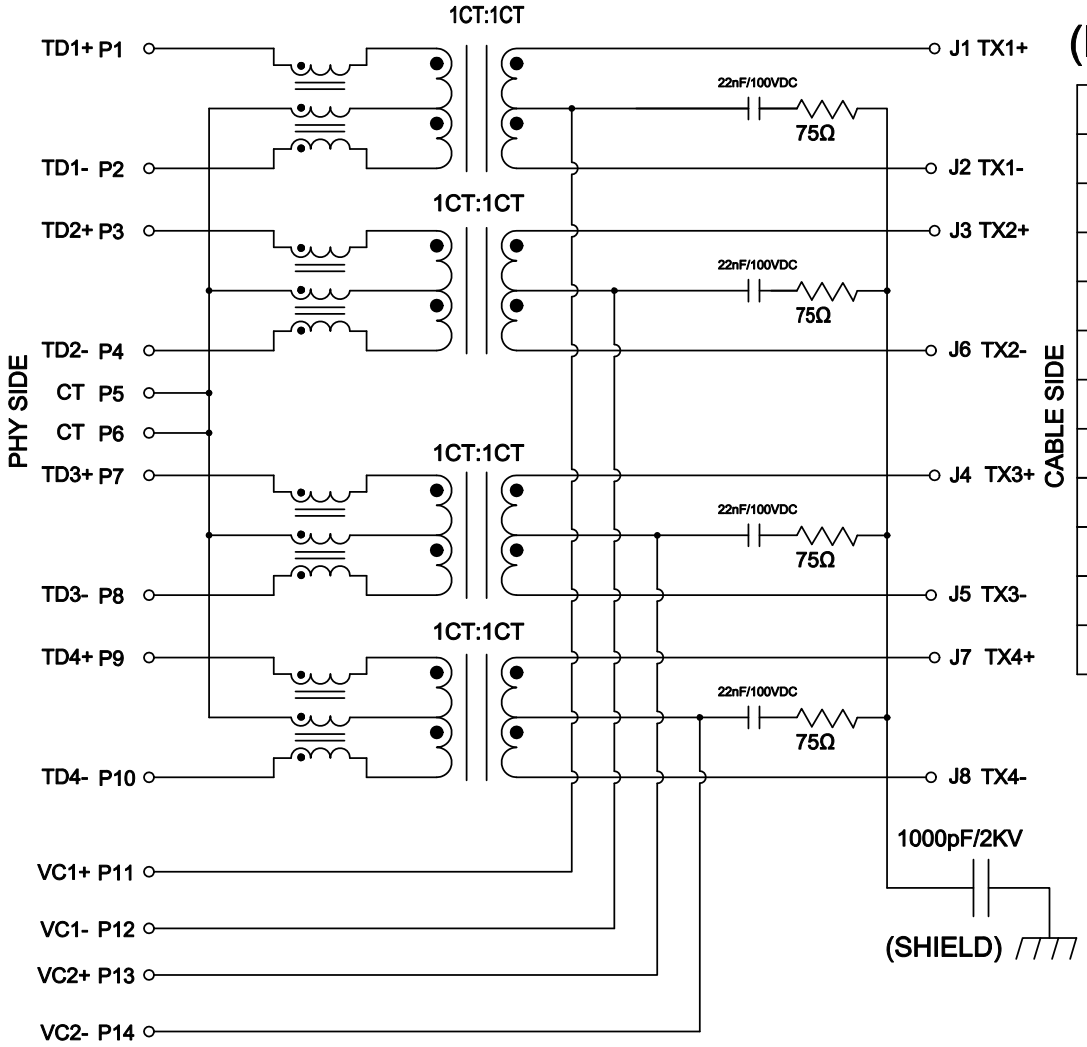
MATERIALS

1.HOUSING:GLASS FILLED LCP UL94V-0(ROHS)
2.CONTACT: PHOSPHOR BRONZE,50-100 MICROINCHES MIN. OVERALL DUCTILE NICKEL UNDERPLATE WITH 6 MICROINCHES GOLD FLASH AT MATING INTERFACE
3.SHIELD:0.2mm THICKNESS WITH BRASS.
4.JACK CAVITY CONFORMS TO FCC RULES AND REGULATIONS PART 68 SUBPART F
5.THE PART IS RECOMMENDDED FOR THROUGH HOLE REFLOW SOLDERING PROCESS PEAK SOLDERING TEMPERATURE IS 260°C MAX,10 SECS MAX.
6.OPERATING TEMPERATURE:0°C TO +95°C. STORAGE TEMPERATURE:-40°C TO +85°C.

产品客户图 Customer Drw				GLGNET	® 深圳市方向电子股份有限公司 SHEN ZHEN GLGNET ELECTRONICS CO. ,LTD.				
未注公差 TOLERANCE UNLESS OTHERWISE SPECIFIED		0.XX	±0.10	Description	RJ45 1X2 Tab_Up/Through Hole/Offset/PIP制程 W/O LED PORT A 2.5GBase-T(UPoE/60W)/PORT B 1000Base-T				
		X.XX	±0.25						
		XX.XX	±0.25						
		X°	±2°						
比例 SCALE	1:1	角法 PROJ.		设计 DESIGN	WANGKG	2022.02.19	品名 TITLE	JRSDBPNA2E809P	
张数 SHEET	1/3	大小 SIZE	A4	校对 CHECKED	DANNY	2022.02.19	料号 ITEM NO.	130076-00211	
单位 UNIT	mm	版本 REV.	A0	核准 APPROVED	BYANG	2022.02.19	图号 DWG NO.		

NO.	ECN NO.	DESCRIPTION	REV.	DRAW	DATE

Schematic(PORT A)



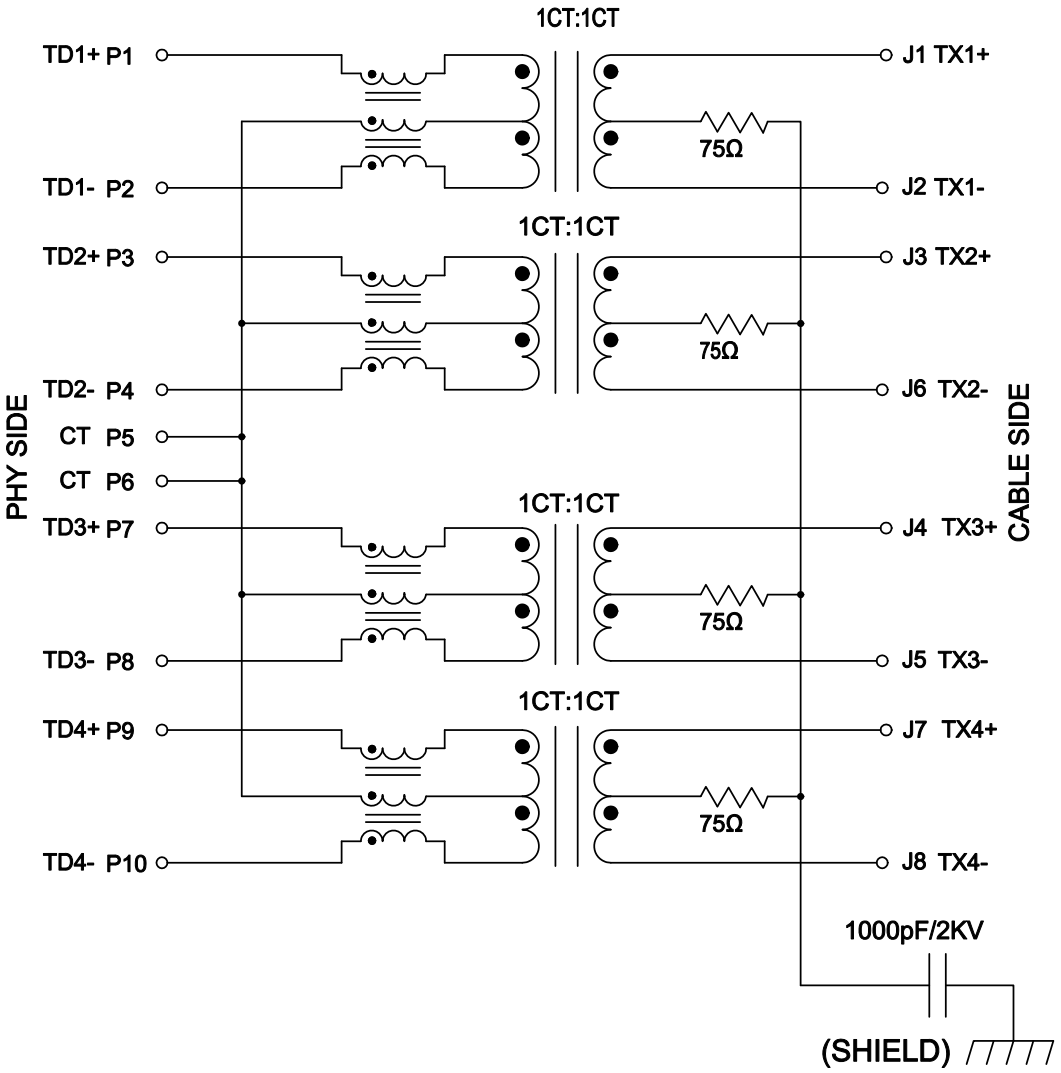
(PORT A/2.5G BASE-T(UPoE))

PARAMETER	SPECIFICATIONS
OPERATING TEMPERATURE	0°C To +95°C
TURNS RATIO	1:1±2%
OPEN CIRCUIT INDUCTANCE(OCL)	120uH MIN@100KHz/100mV With 15mA DC Bias For(CHANNEL1,2,3,4) 180uH MIN@100KHz/100mV With 8mA DC Bias For(CHANNEL1,2,3,4)
INSERTION LOSS(IL)	-1.0dB MAX@1MHz-50MHz; -1.5dB MAX@50MHz-125MHz;
RETURN LOSS(RL) (Z out=100 OHM)	-18dB MIN@1MHz-40MHz; -18+15LOG (f/40MHz)dB MIN@40MHz-250MHz;
CROSSTALK (ADJACENT CHANNELS)	-35dB MIN@1MHz-40MHz; -35+15LOG (f/40MHz)dB MIN@40MHz-125MHz;
COMMON MODE REJECTION RATIO(CMRR)	-30dB MIN@1MHz-200MHz;
COMMON TO DIFFERENTIAL MODE REJECTION(REF)	-35dB MIN@1MHz-125MHz;
DIFFERENTIAL TO COMMON MODE REJECTION(REF)	-40dB MIN@1MHz-10MHz; -28dB MIN@40MHz-100MHz; -23dB MIN@200MHz;
DC CURRENT/VOLTAGE RATING-PSE PINS	720mA MAXIMUM@57VDC(CONTINUOUS)
HI-POT	2250 VDC@60 SECONDS

产品客户图 Customer Drw				GLGNET	® 深圳市方向电子股份有限公司 SHEN ZHEN GLGNET ELECTRONICS CO. ,LTD.				
未注公差 TOLERANCE UNLESS OTHERWISE SPECIFIED	0.XX	±0.10		Description	RJ45 1X2 Tab_Up/Through Hole/Offset/PIP制程 W/O LED PORT A 2.5GBase-T(UPoE/60W)/PORT B 1000Base-T				
	X.XX	±0.25							
	XX.XX	±0.25							
	X°	±2°							
比例 SCALE	1:1	角法 PROJ.		设计 DESIGN	WANGKG	2022.02.19	品名 TITLE	JRSDBPNA2E809P	
张数 SHEET	2/3	大小 SIZE	A4	校对 CHECKED	DANNY	2022.02.19	料号 ITEM NO.	130076-00211	
单位 UNIT	mm	版本 REV.	A0	核准 APPROVED	BYANG	2022.02.19	图号 DWG NO.		

NO.	ECN NO.	DESCRIPTION	REV.	DRAW	DATE

Schematic(PORT B)



(PORT B/1000BASE-T)

PARAMETER	SPECIFICATIONS
OPERATING TEMPERATURE	0°C To +95°C
TURNS RATIO	1:1±2%
INDUCTANCE(OCL)	350uH MIN@100KHz/100mV With 8mA DC Bias
INSERTION LOSS	-1.0dB MAX@0.5MHz-100MHz;
RETURN LOSS (Z out=100 OHM)	-18dB MIN@1MHz-30MHz; -16dB MIN@30MHz-60MHz; -12dB MIN@60MHz-80MHz; -10dB MIN@80MHz-100MHz
CROSSTALK (ADJACENT CHANNELS)	-30dB MIN@1MHz-100MHz;
COMMON MODE REJECTION RATIO	-30dB MIN@0.5MHz-1MHz; -30dB MIN@1MHz-100MHz;
DC CURRENT/VOLTAGE RATING-PSE PINS	2250 VDC@60 SECONDS

产品客户图 Customer Drw				GLGNET	® 深圳市方向电子股份有限公司 SHEN ZHEN GLGNET ELECTRONICS CO. ,LTD.				
未注公差 TOLERANCE UNLESS OTHERWISE SPECIFIED		0.XX	±0.10	Description	RJ45 1X2 Tab_Up/Through Hole/Offset/PIP制程 W/O LED PORT A 2.5GBase-T(UPoE/60W)/PORT B 1000Base-T				
		X.XX	±0.25						
		XX.XX	±0.25						
		X°	±2°						
比例 SCALE	1:1	角法 PROJ.		设计 DESIGN	WANGKG	2022.02.19	品名 TITLE	JRSDBPNA2E809P	
张数 SHEET	3/3	大小 SIZE	A4	校对 CHECKED	DANNY	2022.02.19	料号 ITEM NO.	130076-00211	
单位 UNIT	mm	版本 REV.	A0	核准 APPROVED	BYANG	2022.02.19	图号 DWG NO.		